

3D-Design in Cadence Allegro / OrCAD

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Overview

• Flex

- Cross Section
- Layer Definition
- Zones
- Bend Area
- Interlayer Checks
- Contour Routing
- Visualization
- Cross Hatch Shapes
- Outlook

- Embedded Components
 - Advantages
 - Cross Section
 - Attachment Method
 - Rules Setup
 - Analysis Modes
 - Additional Layers
 - Part Properties
 - Placement
 - Dual Sided Components
 - Manufacturing
 - Documentation
 - 3D Visualization

 Combination Flex and Embedded Components



Personal Introduction

- Holger Schröter
- Studies: Communications Engineering at TU Braunschweig
- Distance control radar at TU Braunschweig
- Development and project management for VCO and frequency synthesizer at Tyco Electronics
- Development of memory modules at Qimonda (Infineon)
- PCB Design Flow und Methodology at Intel
- Application Engineer at FlowCAD





Flexible PCB – Design

4



Flexible PCB – Overview







• Flex

- Permanent flexible
- Based on polyimide
- In most cases a PCB is build in a package twisted or folded
- Can be used for static as well as dynamic applications
- Semi-flex
 - Limited number of bending cycles, bending radius
 - Based on FR4
 - Cost efficient "Flex to Install" solution

- Rigid-flex
 - PCBs with flexible and rigid areas
 - Combination of polyimide and FR4
 - Connection of rigid PCB without cable and connectors
 - Advantages in costs and signal integrity



Cross Section I

• Multi Stackups mode to be enabled under "View"





Cross Section II

• Primary Stackup

Cross Section Editor	(Multi Stackups mode)
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Export Import Edit View Filters

Objects		Тур)es >>	Thickness >>	Ph	ysical >>
# Name	La	yer	Layer Function	mm	Layer ID	Material
*	*	*		*	*	*
	Surfac	e				
SOLDERMASK TOP	P Mask	So	der Mask	0.02		Soldermask
1 TOP	Condu	ctor Co	nductor	0.03	1	Copper
	Dielect	ric Die	lectric	0.2		Polyimide
2 LAYER_1	Condu	ctor Co	nductor	0.02	2	Copper
	Dielect	ric Die	lectric	0.2		Fr-4
3 LAYER_2	Condu	ctor Co	nductor	0.02	3	Copper
	Dielect	ric Die	lectric	0.5		Fr-4
4 LAYER_3	Condu	ctor Co	nductor	0.02	4	Copper
	Dielect	ric Die	lectric	0.2		Fr-4
5 LAYER_4	Condu	ctor Co	nductor	0.02	5	Copper
	Dielect	ric Die	lectric	0.2		Polyimide
6 BOTTOM	Condu	ctor Co	nductor	0.02	6	Copper
SOLDERMASK_BOT	TOM Mask	So	der Mask	0.02		Soldermask
	Surfac	e				

<u>?</u>× cādence

PRIMARY

Surface

TOP Conductor

Dielectric

Dielectric LAYER 2 Conductor

Dielectric LAYER_3 Conductor

Dielectric LAYER_4 Conductor

Dielectric BOTTOM Conductor

Surface

SOLDERMASK BOTTOM Mask

LAYER 1 Conductor

SOLDERMASK TOP Mask



Cross Section III

• Flex Main

	stackups Primary Fle	x Main Flex Stif	fened +						z	
	Objects		Types >>	Thickness >>	PI	hysical >>			IAI	
	објеса	Laver Laver Function Value Laver ID Material							Ž.	
#	Name	Layer	Layer Function	mm	Layerib	Material			Ĥ	
	*	*	*	*	*	*			_ E	1
		Surface	8					Surface		
	COVER_TOP	Mask	Dielectric Coverlay	0.1		Polyimide		COVER TOP Mack		
	ADHESIVE_TOP	Mask	Dielectric Adhesive	0.025		Adhesive Epoxy		COVER_TOP Hask		
5	LAYER_4	Conductor	Conductor	0.02	5	Copper		ADHESIVE_TOP Mask		
		Dielectric	Dielectric	0.2		Polyimide	5	LAYER_4 Conductor		
	ADHESIVE_BOTTOM	Mask	Dielectric Coverlay	0.025		Adhesive Epoxy		Dielectric		
	COVER_BOTTOM	Mask	Dielectric Coverlay	0.1		Polyimide				
		Surface						ADHESIVE_BOTTOM Mask		
								COVER_BOTTOM Mask		
								Surface		

Flex
 Stiffened

All s	stackups Primary Fle	ex Main Flex Stiff	ened +		-				4ED		
	Objects		Types >>	Thickness >>	Ph	nysical >>			E E		
		Laver	Laver Function	Value		Material			41.		
#	Name	Layer	Layer runction	mm	Layerib	Material			5		
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		Surface						1	Η	1	
	COVER_TOP	Mask	Dielectric Coverlay	0.1		Polyimide		Surface			
	ADHESIVE_TOP	Mask	Dielectric Adhesive	0.025		Adhesive Epoxy		COVER TOP Mask			
5	LAYER_4	Conductor	Conductor	0.02	5	Copper		ADHESIVE TOP Mask			
		Dielectric	Dielectric	0.2		Polyimide	5	LAYER 4 Conductor			
	ADHESIVE_BOTTOM	Mask	Dielectric Coverlay	0.025		Adhesive Epoxy		Dielectric			
	COVER_BOTTOM	Mask	Dielectric Coverlay	0.1		Polyimide		ADHESIVE BOTTOM Magh			
	STIFENER	Mask	Dielectric Coverlay	5		Aluminum		COURD POTTON Moak			
		Surface						COVER_BOITON MASK			



Cross Section IV

- Layer details can be edited in different stackups
 - Physical details
 - Embedding
 - Signal Integrity

- -	obb occurrin Editor (Francioca	chaps model)												
Expor	t Import Edit View Filters													
All	stackups Primary Flex Ma	ain Flex Stiffen	ed +											
	Objects	Тур	es >>	Thickness >>			Physic	cal <<			Embedded >>	Sign	al Integrity >>	د
	Objects	Lavor	Lavor Eunction	Value	Lavor ID	Matorial	Negative	No Fillot	Unused Pin	Unused Via	Emboddod Status	Conductivity	Dielectric	SUlanoro
#	Name	Layer	Layer Function	mm	Layer ID	Wateria	Artwork	No Fillet	Suppression	Suppression	Linbedded Status	mho/cm	Constant	Singhore
*	*	*	*	*	*	*	*	* * *		*	*	*	*	*
		Surface											1	
	SOLDERMASK_TOP	Mask	Solder Mask	0.02		Soldermask						0	3.7	
1	ТОР	Conductor	Conductor	0.03	1	Copper					Not embedded	595900	4.5	
		Dielectric	Dielectric	0.2		Polyimide						0	4.3	
2	LAYER_1	Conductor	Conductor	0.02	2	Copper					Not embedded	595900	4.5	
		Dielectric	Dielectric	0.2		Fr-4						0	4.5	
3	LAYER_2	Conductor	Conductor	0.02	3	Copper					Not embedded	595900	4.5	
		Dielectric	Dielectric	0.5		Fr-4						0	4.5	
4	LAYER_3	Conductor	Conductor	0.02	4	Copper					Not embedded	595900	4.5	
		Dielectric	Dielectric	0.2		Fr-4						0	4.5	
5	LAYER_4	Conductor	Conductor	0.02	5	Copper					Not embedded	595900	4.5	
		Dielectric	Dielectric	0.2		Polyimide						0	4.3	
6	BOTTOM	Conductor	Conductor	0.02	6	Copper					Not embedded	595900	4.5	
	SOLDERMASK_BOTTOM	Mask	Solder Mask	0.02		Soldermask						0	3.7	
		Surface											1	

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Layer Definition

• Add Layers dialog to define Stackup in "All Stackups View"

🕏 Add Layers		?>
Count of new layers: 1		Name prefix:
New Layer(s) position		
Above Conductor TOP	C Below Conductor TOP	
Note: Adding Conductor or Plane layers will add Diel	ectric layers around each new Etch laye	yer.
Layer type:	Layer function:	Layer material:
Conductor Dielectric Plane Mask Ste-defined Mask Layers Cover Top Cover Top Adhesive Bottom Cover Bottom Cover Bottom Cover Bottom Cover Bottom Cover Bottom Coverlay Top Enepig Top Enepig Top Enepig Top Enepig Top Enepig Top Gold Hard Top Gold Soft Top Immersion Silver Top Immersion Silver Top Silver Ink Top Soldermask Top Silver Ink Top Soldermask Top Soldermask Top Stiffener Top Stiffener Matal Top Soldermask Top Stiffener Metal Top Soldermask	Capacitive Coating Conductive Coating Non Conductive Conductive Adhesive Conductive Film Conductive Fol Dielectric Adhesive Dielectric Coverlay Dielectric Coverlay Dielectric Prepeg Resistive Silkscreen Solder Mask Solder Paste I layer wll be added above selet * Type: Mask. * Name: COVERLAY_TOP * Function: Dielectric Coverlay * Material: Polyimide.	Adhesive Acrylic Adhesive Epoxy Adhesive Thermoset Air Bt Epoxy Carbon Ink 1ml Carbon Ink 1ml Carbon Ink 2ml Conformal Coat Cyanate Ester E Cyanate Ester S Epoxy Ink Thermoset Epoxy Ink Uv Cure Epoxy Resin High-dk Epox Resin High-
···· Coverlay Bottom ···· Emi Shield Bottom	▼	Add Exit



Site Setup

- Mask Layer Site File ("Edit / Site File")
- Useful due to limitless combinations of materials

🗯 Mask Layer Subclass site f	ile editor.			<u>? ×</u>
Site File Name: D:/Work/Proje	ekte/site_172/pcb/masklayersitefile.xml		Open	Save As
Function	Name	Class Name	Default Material]
Dielectric Adhesive	ADHESIVE_TOP	Rigid Flex	Adhesive Epoxy	
Dielectric Coverlay	COVER_TOP	Rigid Flex	Polyimide	
Dielectric Coverlay	ADHESIVE_BOTTOM	Rigid Flex	Adhesive Epoxy	Add
Dielectric Coverlay	COVER_BOTTOM	Rigid Flex	Polyimide	Delete
Coating Conductive	STIFENER	Rigid Flex	Aluminum	
				ОК
				Cancel

• Default location: MATERIALPATH



Zones



defined in Zone Manager

F	Zone M	anager								ı ×
	Select	Name	Stackup		Start Layer	Stop Layer	Constraint Reg		Room	
		MAIN_PCB	PRIMARY	Ŧ	ТОР	воттом		-		•
		FLEX_1	FLEX_1	•	INNER1	INNER2	FLEX	•		
		FLEX_1_STIFFENER	FLEXI_STIFFENED	۲	INNER1	INNER2	FLEX	•	RF-AMP	
		FLEX_2	FLEX_2	۲	INNER1	INNER2	FLEX	•		



Bend Area

💓 Edit Bend A	\rea	? ×									
Bend name: BE	END_3	-									
Bend line start											
X: 22	2.350 Y: 52.672										
Bend line end											
X: 35	5.900 Y: 66.000										
Bending Paran	neters										
Inner side:	Тор	•									
Inner radius:	Inner radius: 6.000										
Angle:	75.000										
Order:	Order: 3										
Bend Area Opt	tions										
✓ Via keepo	ut										
Oversize: 1	1.000										
Package k	eepout										
Oversize: 2	2.000										
Apply	Close Delete bend Help										

- Bends are defined by following parameters:
 - Position
 - Direction
 - Radius
 - Angle
 - Additional keepouts





Interlayer Checks – Constraint Manager

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Interlayer Checks – Rule Examples

- DRC engine designed to check
 - Mask layer to mask layer geometry
 - Mask layer to surface metal
- Layer selection GUI
 - Matrix of applicable subclasses
 - Filtering capabilities
 - Comment field

- Gaps:
 - Coverlay to pad
 - Mask to pad
 - Precious metal to coverlay
 - Bend area/line to stiffener, component, pin, and via
- Minimum overlap, e.g.:
 - Transition zone must overlap bend area by 15 mils
- Inside Rule:
- (Layer 1) inside (layer 2)
- Geometry on one subclass must be contained within the geometry of another subclass geometry



Contour Routing

 Simplified routing of traces along rounded contour of flex boards





Cross Hatch Shapes

- Cross Hatch (Xhatch) shapes are common with Flex PCBs
 - Lighter in weight
 - Adheres better, less prone to cracking at bend areas
- Dynamic cross hatch is supported by shape-add feature

Options Active Class and Subclass: Etch Top Top Shape Fill Type: Dynamic crosshatch Defer Cavity Dynamic copper Dynamic crosshatch Assign no Static solid Dummy Static crosshatch Unfilled Shape grid: Current grid Shape Creation Draw Rectangle Place Rectangle Width (W):
Active Class and Subclass: Etch Top Shape Fill Type: Dynamic crosshatch Defer Cavity Dynamic copper Dynamic crosshatch Assign n' Static solid Dummy Static crosshatch Unfilled Shape grid: Current grid Shape Creation One Draw Rectangle Place Rectangle Width [W]: 5650.0
Draw Rectangle Place Rectangle Width (W):
 Draw Rectangle Place Rectangle Width (W): 5650.0
Width (W): 5650.0
width (w):



Visualization / Interfaces

Interactive 3D Canvas



• Step export of complete design



Outlook

- Visualization of different stackups in Interactive 3D Canvas
 - Currently only the primary stackup is displayed

- Bending in Interactive 3D Canvas
 - In preparation, planned for this year



Embedded Components

20



Advantages

- Miniaturization
 - Significant reduction of form factor
- Electrical performance
 - E.g. passives closer to active components
- Protection of components
- Less bending stress
- EMI protection
- IP-protection
 - Internal die has no marking
- Compatible to traditional SMT processes





Cross Section

- Not embedded: Default, no embedded placement on this layer
- Body up: Components can be placed on this layer with body up
- Body down: Components can be placed on this layer with body down
- Protruding allowed: Components can break through this etch layer

💐 Cr	oss Section Editor									? ×
Expor	t Import Edit View	Filters								cādence
Pri	nary									KX
	Objects		Types >>	Thickness >>	Ph	ysical >>	Embedded >>			MA
	Objects	Laver	Laver Function	Value	Laver ID	Material	Embedded Status			PRJ
#	Name	201701	Lujorrunouon	mm					Surface	
_	*	*	*	*	*	*	*	- 1	TOD Conductor	
		Surface						*	TOP Conductor	
1	ТОР	Conductor	Conductor	0.03	1	Copper	Not embedded	_	Dielectric	
		Dielectric	Dielectric	0.2		Fr-4		2	LAYER 1 Conductor	
2	LAYER_1	Conductor	Conductor	0.03	2	Copper	Body down		Dielectric	
		Dielectric	Dielectric	0.4		Fr-4			Dicicotiic	
3	LAYER_2	Conductor	Conductor	0.03	3	Copper	Not embedded	3	LAYER_2 Conductor	
		Dielectric	Dielectric	0.5		Fr-4			Dielectric	
4	LAYER_3	Conductor	Conductor	0.03	4	Copper	Protruding allowed	4	LAYER 3 Conductor	
		Dielectric	Dielectric	0.4		Fr-4				
5	LAYER_4	Conductor	Conductor	0.03	5	Copper	Body up	-	Dielectric	
		Dielectric	Dielectric	0.2		Fr-4	Not embedded	5	LAYER_4 Conductor	
6	BOTTOM	Conductor	Conductor	0.03	6	Copper	Body up		Dielectric	
		Surface					Body down	6	BOTTOM Conductor	
							Protruding allowed			
									Surface	



Attachment Method

- Direct attach:
 - Standard process
 - Component is directly soldered to inner layer
- Indirect attach
 - Components are mounted in substrate
 - Contacted by single layer µVias

🗯 Cr	oss Section Editor							? ×		
Expo	rt Import Edit View	Filters								cādence
Pri	mary								х	
		Thickness >>	Ph	ysical >>	Embed	ded <<	1		MAR	
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#	Name	mm	*	*	*	*	-	Surface		
_				- - - -			1	TOP Conductor		
1	ТОР	0.03	1	Copper	Not embedded		-	Dielectric		
		0.3		Fr-4			2	LAYER 1 Conductor		
2	LAYER_1	0.03	2	Copper	Body down	Direct attach		Dielectric		
_		0.5		Fr-4			2	TAVED 2 Conductor		
3	LAYER_2	0.03	3	Copper	Not embedded			LATER_2 Conductor		
4		0.03	4	FF-4	Protruding allowed		1	Dielectric		
4	LATER_3	0.05	4	Er A	Frouturing anowed		4	LAYER_3 Conductor		
5	LAYER 4	0.03	5	Copper	Body up	Indirect attach		Dielectric		
		0.3	_	Fr-4			5	LAYER_4 Conductor		
6	BOTTOM	0.03	6	Copper	Not embedded			Dielectric		
							6	BOTTOM Conductor		
								Surface		
4						•				
						<u>_</u>	1			

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23



Indirect Attach Vias

- Property EMB_VIA_CONNECT_PADSTACK
 - Specifies the name of the via padstack to be used for connecting the embedded component to the etch layer (indirect attach)
 - Has to be specified at drawing level of a symbol

🔜 Edit Property		_ 🗆 🗙
Available Properties	Delete Property Version_Id Pkgdef_Step_File Pkgdef_Step_Transformation Emb_Via_Connect_Padstack	Value
OK Cancel Help	Reset Apply Show->	

Find By Name	
Drawing 💌	Name
>	More



Redundant Vias

• Possibility to define in Padstack Editor

🚀 Pad Editor: EMBEDD File View Help	D_VIA_VERTICAL (D:/Work/Projekte/17_2/FED_2017_04_12)	_□× ādence
2D Top Padstack View	Start Drill Secondary Drill Drill Symbol Drill Offset Design Layers Mask Layers Options Summer Drill hole Hole type: Circle Image: Circle Im	mary
	Finished diameter: 0.0900 + Tolerance: 0.0000	
2D Padstack Side Views	- Tolerance: 0.0000 Drill tool size: Image: Compare the size of the	
	Hole plating Hole/slot plating:	
	Define the drill rows and columns	
	Number of drill rows: 2	
	Number of drill columns: 1 Clearance between columns: 0.0500	
	Clearance between rows: 0.0250	
	Drills are staggered	
Side Front		
SMD Pin Units: Millime	r 💌 Decimal places: 4 💌	

25



Rules Setup

- 1. Height buffer to next etch layer
- 2. Minimal gap to next cavity before merging
- 3. Creates a via keepout based on placebound
- 4. Package to cavity spacing, same as under Constraints / Modes / Design Options
- 5. Gap between etch layer and component pad
- 6. If padstack for embedding is not defined within component, this padstack will be used
- 7. Route keepout around cavity, when components protrudes





Analysis Modes

- Package to cavity spacing, same as in Cross Section Editor
- Check package height + buffer to next etch layer
- Maximal area of a cavity
- Maximal number of components in one cavity

Design Name Value On Off Batch Physical Spacing Image: Spacing <	🔜 Analysis Modes				? ×
Package to place keepin M L L Package to place keepout M L L Package to place keepout M L L Package to room M L L Package to room M L L Package to cavity spacing 0.2500mm M L Package height to layer Max cavity area Max cavity area L Max cavity component count 10 M L L	Analysis Modes	Name Mark All Constraints General Soldermask Acute Angle Detection Package Package Package to package Package to place keepin Package to place keepout Package to room Package to cavity spacing Package height to layer Max cavity area Max cavity component count	Value 0.2500mm 25.0000mm 10		Patch Batch G G G G G G G G G G G G G

28 AD.com 50

Additional Layers

• Required additional layers are auto generated:

💥 Color Dialog		
Layers Nets Display	Favorites Visibility Pane]
Filter layers:		
Stack-Up	All	EmbGeo
Board geometry	Assembly_Layer_1	
Package geometry	Assembly_Layer_4	
Components	Dfa_Bound_Layer_1	
Drawing format	Dfa_Bound_Layer_4	
Rigid flex	Display_Layer_1	
Bond wire profiles	Display_Layer_4	
Surface finisnes	Pastemask_Layer_1	
	Pastemask_Layer_4	
	Place_Bound_Layer_1	
	Place_Bound_Layer_4	
	Soldermask_Layer_1	
	Soldermask_Layer_4	

Color Dialog												
Layers Nets Display	Favorites Visibility Pa	ine										
Filter layers:												Glo
Stack-Up Areas Geometry	All		ा र	ol	DevT	ype	Cmp I	oVal	UserF	Part	Refl	Des
Board geometry	Assembly_Bottom				•		V		~		•	
Package geometry Embedded geometry	Assembly_Embedded				7		V		▼		~	
Components	Assembly_Layer_1	V			2		V		✓		~	
Dev type	Assembly_Layer_4				P		V		~		>	
Ref des	Assembly_Top	~	•		P		Y		~		~	
User part	Display_Bottom	~			P		V		~		>	
Manufacturing Drawing format	Display_Embedded		•		7		~		~		~	
Rigid flex	Display_Layer_1				P		Y		Y		>	
Bond wire profiles	Display_Layer_4		•		v		V		~		~	
····· Surface finishes	Display_Top				2		V		V		•	
	Silkscreen_Bottom	~	7		2		~		~		•	
	Silkscreen_Top				2		V		V		•	





Part Properties I

- Embedded Placement is triggered by Property "Embedded_Placement":
 - Required: Component has to be embedded, no placement on outer layer allowed
 - Optional: Component can be embedded
 - External Only: Placement on outer layer only
- Can already be done at schematic level

🔳 Edit Property			
Available Properties	Delete Property	Value	Main Show Properties
Bom_Ignore Comment Component_Weight Connector_Signal_Model Dense_Component Ecset_Mapping_Tag Emb Indirect Via Suppress Embedded_Placement Emc_Comp_I ype Emc_Critical_Ic Fix_All Fixed Mame:	Embedded_Placement	REQUIRED OPTIONAL EXTERNAL_ONLY	<pre></pre>
OK Cancel Help	Reset Apply Show->	•]	i i i i i i i i i i i i i i i i i i i
Select popup in the value field, or leave blank	kto ignore.		



Part Properties II

- Handling in Constraint Manager
- Important for Dual Sided Components
 - Embedded Placement Property required to place

🚰 Allegro Constraint Manager (con	Allegro Constraint Manager (connected to Allegro PCB Designer 17.2) [embedded_1] - [Properties / Component / Component Properties]										
📕 File Edit Objects Column View A	nalyze A	udit	Tools Window	v Help							
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Electrical								Embedded		Plac	
+ Physical			, c	Dbjects							
🔐 Spacing	Type	S		Name		Layer	Status	Attach	Placement	Tag	
🖳 Same Net Spacing	*	*	*			*	*	*	*	*	
Assembly	Prtl	Ť	R620						8		
Properties	PrtD		⊟ RES_H_4>	(_RES_RS4N_DISCRET	'E_22_F						
	Prtl		R500						8		
🖻 🛅 Component	Prtl		R501						OPTIONAL		
Component Properties	Prtl		R502			LAYER_1	BODY_DOWN	DIRECT_ATTACH	OPTIONAL		
General	Prtl		R503			LAYER_4	BODY_UP	INDIRECT_ATTACH	OPTIONAL		
Thermal	Prtl		R512						8		
	Prtl		R513						8		
	Prtl		R514						8		
Reuse	Prtl		R515						8		
⊡	Prtl		R516						8		
	Prtl		R517				~ <u>~</u> ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	400000000000000000000000000000000000000	8		



Placement

Manual:



Quickplace:

🕺 Quickplace 📃 🗌 🗙
Placement filter
Place by property/value Embedded_F Optional
○ Place by room
○ Place by part number
Place by net name *
O Place by net group name ★ …
Place by schematic page number
Place all components
Place by associated components
Place by refdes
Place by REFDES Type: IC IO Discrete Refdes: C Include Include C Exclude Include Include Number of pins: Min: 0 Max: 0
Placement position Place by partition Place associated components on parent pins
O By user pick Select origin
Around package keepin
Edge



Cases

1. Top

- 2. Layer_1, Direct attach
 - DRC: Package Height to Layer Spacing
- 3. Layer_3, Protruding allowed
- 4. Layer_4, Indirect attach



\$ 0	ross Section Editor									? ×
Exp	ort Import Edit View	Filters								cādence
P	rimary								ж	
-	Objects	Thickness >>	Ph	ysical >>	> Embedded <<		[IMAR	
_	Nama	Value	Layer ID	Material	Embedded Status	Attach Method	-		- ^{BB}	
*	* Name	*	*	*	*	*		Surface		
							1	TOP Conductor		
1	ТОР	0.03	1	Copper	Not embedded			Dielectric		
		0.3		Fr-4			2	LAYER 1 Conductor		
_2	LAYER_1	0.03	2	Copper	Body down	Direct attach	4	_ Dielectric		
		0.5	2	Fr-4	N / 1 11 1		3	LAVER 2 Conductor		
3	LAYER_2	0.03	3	Copper	Not embedded		1	DATER_2 CONDUCCOI		
4	LAYER 3	0.03	4	Copper	Protruding allowed			Dielectric		
		0.5		Fr-4	r roudung uno nou		4	LAYER_3 Conductor		
5	LAYER_4	0.03	5	Copper	Body up	Indirect attach		Dielectric		
		0.3		Fr-4			5	LAYER_4 Conductor		
6	воттом	0.03	6	Copper	Not embedded		1	Dielectric		
							6	BOTTOM Conductor		
								Surface		
						•				
							4			



Dual Sided Components

- Allegro PCB Editor supports use of dual-sided contact components
- Benefits: Reduction of vias
- Requirement:
 - "DUAL_SIDED_COMPONENT" Property on Symbols (.dra) defined on drawing level
 - Padstacks must have begin and end layer pad
 - "EMBEDDED_PLACEMENT = OPTIONAL or REQUIRED" on Component
 - No placement of dual sided components allowed on outer layers
- All PCB Editor embedded setup methodologies are fully supported:
 - Direct / indirect attach
 - Typically indirect attach is used
 - Body up / body down







Vertical Components

- "Special case" of Dual Sided Components
- Mapped to different padstacks with Begin or End Layer pad





PCB Manufacturing

Film Control Form Film Control General Parameters Available films Domain Selection BOTTOM	Create Missing Films	 Embedded layers can be use for Film generation
LAYER_1 LAYER_2 LAYER_3 LAYER_3 LAYER_4 CAVITY_2_3 CAVITY_2_3 CAVITY/LAYER_2 CAVITY/LAYER_1 CAVITY/LAYER_1 CAVITY/LAYER_1		NC Drill supports single layer vias for indirect attach
EMBEDDED GEOMETRY/ASSEMBLY_LAYER_1	Datei Bearbeiten Format Datei Bearbeiten Format [LEADER: 12 ;HEADER: ;CODE : ASCII ;FILE : embedded_1 ;FILE : embedded_1 ; Holesize 1. = 0 % G90 X4338750Y0975000 X4338750Y0975000 X4351250Y0925000 X4351250Y0825000 X4351250Y0825000 X4351250Y0825000 X4461250Y0825000 X4461250Y0825000 X4461250Y0875000 X4461250Y0875000 X4461250Y0925000 X4461250Y0975000 X	Ansicht ?

Assembly

• Reports feature in Allegro PCB Editor support Embedding

	А	В	С	D	E	F	G	Н
1	Allegro Report							
2	D:/Work/Pr	ojekte/17_2/FED_	2017_04_12/embedded	_1.brd				
3	Fri Mar 24 1	12:55:29 2017						
4								
5	REFDES 💌	PART_NAME	EMBEDDED_LAYER	EMBEDDED_STATUS	EMBEDDED_ATTACH	SYM_CENTER_X	SYM_CENTER_Y	SYM_ROTATE
260	R506	RES_V				21.000	10.000	0.000
384	R502	RES_H_4x	LAYER_1	BODY_DOWN	DIRECT_ATTACH	39.000	9.000	0.000
385	R503	RES_H_4x	LAYER_4	BODY_UP	INDIRECT_ATTACH	44.000	9.000	0.000
386								

- IPC2581
- ODB++ Version 9.1



Documentation

* SURFACE - AIR 0 MM LI TOP CONDUCTOR - COPPER 0.03 MM NOT_EM * DIELECTRIC - FR-4 0.3 MM L2 LAYER I CONDUCTOR - COPPER 0.03 MM BO	Cross Section Chart contains embedding information			
* DIELECTRIC - FR-4 0.5 MM	Drill Chart supports single			
L3 LAYER_2 CONDUCTOR - COPPER 0.03 MM NO	L3 LAYER_2 CONDUCTOR - COPPER 0.03 MM NOT EMBEDDED			attaon
* DIELECTR[C - FR-4 0.6 MM -	DRILL ALL FIGURE F	4 to LAYER MILLIMETERS PLATED	YER_4 ERS DQTY	
		0.1	PLAIED	16
L4 LAYER_3 CONDUCTOR - COPPER 0.03 MM PR				
* DIELECTR[C - FR-4 0.5 MM			CAD.co	
L5 LAYER_4 CONDUCTOR - COPPER 0.03 MM BO				
* DIELECTRIC - FR-4 0.3 MM			K.Flo	
L6 BOTTOM CONDUCTOR - COPPER 0.03 MM NOT * SURFACE - AIR 0 MM				
DESIGN CROSS SECTION CHART TOTAL THICKNESS 2 38 MM				



3D Visualization







Combination Flexible PCB and Embedded Components

39

FlowCAD

? ×

Combination Flex / Embedded Components

鱨 Cross Section Editor (Multi Stackups mode)

Export Import Edit View Filters

All	All stackups Primary Flex N		Flex Main Flex S	Stiffener +					
Objects			Types	ypes Thickness	Material	Primary	Flex Main	Flex	Add Stacku
#		Name	Layer	mm				Junener	
*	*		*	*	*	*	*	*	*
			Surface						
	COVERLA	AY_TOP	Mask	0.2032	Polyimide	v	V	N	1
	ADHESIV	E_TOP	Mask	0.025	Adhesive Epoxy	V		V	
	SOLDER	MASK_TOP	Mask	0.015	Soldermask	V			1
1	TOP		Conductor	0.055	Copper				
			Dielectric	0.15	Fr-4	v			1
2	GND1		Plane	0.03	Copper				
			Dielectric	0.25	Fr-4	v			1
3	11		Conductor	0.033	Copper			N	
			Dielectric	0.2032	Polyimide	v	V		
4	POW1		Conductor	0.033	Copper			~	1
			Dielectric	0.2032	Fr-4	v			1
5	GND2		Conductor	0.033	Copper				
			Dielectric	0.2032	Polyimide	v			1
6	12		Conductor	0.033	Copper				
			Dielectric	0.25	Fr-4	v			1
7	POW2		Plane	0.03	Copper				
			Dielectric	0.15	Fr-4	<u> </u>			1
8	BOTTOM		Conductor	0.055	Copper				
	SOLDER	MASK BOTTO	M Mask	0.015	Soldermask	v			1
	ADHESIV	E_BOTTOM	Mask	0.025	Adhesive Epoxy	•	v	V	
	COVERL	AY_BOTTOM	Mask	0.2032	Polyimide	▼	v	v	
	STIFFEN	R_BOTTOM	Mask	5	Ptfe			v	1
			Surface				v	.	

Lock Embedded layers setup Unused pads suppression Refresh materials Info

16 mm

Total thickness:	7.198 mm	
Total thickness wi	1.7116 mn	
Layers:	15	
Conductor:	6	
Plane:	2	
Mask:	7	



Help

Kontakt zu FlowCAD

Für weitere Fragen und Informationen stehen wir gerne zur Verfügung

Please don't hesitate to contact us

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FlowCAD







42



Backup





Flex Example



44



Inter-Layer Design Rule Checks Rigid-Flex

45

- DRC engine designed to check
 - Mask layer to mask layer geometry
 - Mask layer to surface metal
- Allows checks for
 - Coverlay to pad checks
 - Mask to pad checks
 - Precious metal to coverlay
 - Bend area/line to stiffener, component, pin, and via
- Layer selection GUI
 - Matrix of applicable subclasses
 - Filtering capabilities
 - User defined DRC 2nd letter ("I" fix first character)
 - Comment field



46



Inter Layer Check Gap Rule

- DRC verifies geometry spacing between subclasses
- Example:
 - Vias, pins and conductors must have 30 mils spacing from Outline





Inter Layer Check Gap Rule





Inter Layer Check Overlap Rule

- Specifies a minimum overlap of two geometries on different subclasses
- Example:
 - Transition zone must overlap bend area by 15 mils
 - Special rules apply in transition zone

Bend Area



Proper Coverlay

Clearances

Inter Layer Check Inside Rule

- (Layer 1) inside (layer 2)
- (Layer 2) inside (layer 1)
- Geometry on one subclass must be contained within the geometry of another subclass geometry

DRC Violation Coverlay on PAD